

WHAT IS CLAIMED IS:

- 1 1. A storage device, comprising:
 - 2 two random access memories each having at least
 - 3 2^{N-1} locations for storing data at respective addresses, N
 - 4 being an integer greater than 1, a data input connected to
 - 5 a data source, a command input, an address input and an
 - 6 output;
 - 7 multiplexing means having first and second data
 - 8 inputs respectively connected to the data outputs of the
 - 9 two memories, a third data input connected to the data
 - 10 source and an output reproducing data present at one of
 - 11 said first, second and third data inputs, selected by
 - 12 switching signals;
 - 13 a controller for issuing electrical signals,
 - 14 within successive time intervals, on controller's outputs
 - 15 including two access command outputs respectively connected
 - 16 to the command inputs of the two memories, two address
 - 17 outputs respectively connected to the address inputs of the
 - 18 two memories and at least a switching command output for
 - 19 issuing said switching signals; and
 - 20 means for sampling the output of the multiplexing
 - 21 means at the beginning of each time interval and producing
 - 22 output data of the device,

23 wherein the controller is set up for issuing, in
24 the course of two consecutive sequences of 2^N time
25 intervals:

26 on each of the two access command outputs, and
27 for at least time intervals distinct from the boundaries
28 of the two sequences, alternate read and write access
29 commands, a write access command being issued on one of
30 said access command outputs while a read access command is
31 issued on the other access command output and vice versa;

32 on each of the two address outputs, increasing
33 addresses during one of the two sequences and decreasing
34 addresses during the other sequence, such that, for at
35 least time intervals distinct from the boundaries of the
36 two sequences, the address input of each memory receives
37 the same address in the course of two consecutive time
38 intervals of each sequence during which the command input
39 of said memory receives a read access command and then a
40 write access command; and

41 on each switching command output, switching
42 signals set so that in the course of each sequence, the
43 sampling means produce data originating from the source in
44 a reverse chronological order from the chronological order
45 of arrival of said data from the source.

1 2. The device according to Claim 1, wherein, during
2 at least one time interval at a boundary of each sequence,
3 the switching signals are issued so that the output of the
4 multiplexing means reproduces data present at said third
5 data input.

1 3. The device according to Claim 1, wherein the
2 controller is set up for coding the addresses of each
3 memory over N-1 bits

1 4. The device according to Claim 1, wherein the
2 means for sampling the output of the multiplexing means
3 include a flip-flop D.

1 5. The device according to Claim 1, wherein the two
2 memories are deferred read memories, the data read in each
3 memory being produced at the output of said memory during
4 the time interval immediately following the time interval
5 during which the command input of said memory receives a
6 read access command and the address input of said memory
7 receives an address.

1 6. The device according to Claim 1, wherein the
2 multiplexing means include:
3 a first multiplexer having:
4 a switching command input connected to a first
5 switching command output of the controller,
6 first and a second data inputs connected
7 respectively to the outputs of the two memories, and
8 an output reproducing the signals from the first
9 or second input of said first multiplexer according to a
10 first switching signal applied to the command input of said
11 first multiplexer; and
12 a second multiplexer having:
13 a switching command input connected to a second
14 switching command output of the controller,
15 first and second data inputs connected
16 respectively to the data source and to the output of the
17 first multiplexer, and
18 an output reproducing the signals from the first
19 or second input of said second multiplexer according to a
20 second switching signal applied to the command input of
21 said second multiplexer.

1 7. The device according to Claim 6, wherein the
2 controller is set up so that the first switching signal and
3 the access command issued by the controller to one of the
4 two memories are identical binary signals, for at least
5 time intervals distinct from the boundaries of the two
6 sequences.

1 8. The device according to Claim 6, wherein the two
2 memories are deferred read memories, the data read in each
3 memory being produced at the output of said memory during
4 the time interval immediately following the time interval
5 during which the command input of said memory receives a
6 read access command and the address input of said memory
7 receives an address, and wherein the controller comprises:

8 a cyclic counter of the time intervals of the two
9 consecutive sequences, set up to produce a number over $N+1$
10 bits, between 0 and $2^{N+1}-1$, for counting the time interval
11 in progress;

12 means for generating at a first access command
13 output connected to a first of the two memories a first
14 binary access command opposite to the least significant bit
15 of the count number of the time interval in progress,

16 during the time intervals respectively numbered from 0 to
17 2^N-3 and from 2^N to $2^{N+1}-3$;

18 means for generating the second access command
19 at a second access command output connected to the second
20 of the two memories in the form of the least significant
21 bit of the count number of the time interval in progress,
22 during the time intervals respectively numbered from 0 to
23 2^N-2 and from 2^N to $2^{N+1}-2$;

24 means for producing, during each time interval,
25 a first partial time interval count number over N-1 bits,
26 equal to the count number for the time interval in progress
27 from which the most significant bit and the least
28 significant bit have been removed;

29 means for generating at a first address output
30 connected to the address input of said first memory an
31 address equal to the first partial count number during the
32 time intervals respectively numbered from 0 to 2^N-3 , and
33 equal to $2^{N-1}-2$ from which the first partial count number is
34 subtracted during the time intervals respectively numbered
35 from 2^N to $2^{N+1}-3$;

36 means for producing, during each time interval,
37 a second partial time interval count number over N-1 bits,
38 equal to the count number for the time interval in progress

39 to which 1 is added, then from which the most significant
40 bit and the least significant bit have been removed;

41 means for generating at a second address output
42 connected to the address input of said second memory an
43 address equal to the second partial count number during the
44 time intervals respectively numbered from 0 to 2^N-2 , and
45 equal to $2^{N-1}-1$ from which the second partial count number
46 is subtracted during the time intervals respectively
47 numbered from 2^N to $2^{N+1}-2$;

48 means for generating at the first switching
49 command output the first switching signal in the form of
50 a binary signal opposite to said first access command;

51 means for generating at the second switching
52 command output the second switching signal in the form of
53 a binary signal equal to 1 when the count number for the
54 time interval in progress, reduced to the N least
55 significant bits, is equal to 2^N-1 , and equal to 0
56 otherwise;

57 each of the two memories being in write or read
58 access mode when the corresponding access command is equal
59 to 0 or 1, respectively;

60 the first and second multiplexer each being set
61 up to instantaneously reproduce at the output of said

62 multiplexer a signal applied to the first or second input
63 of said multiplexer, when the switching signal applied to
64 the command input of said multiplexer is equal to 0 or 1,
65 respectively.

1 9. The device according to Claim 8, wherein:

2 the means of the controller for generating the
3 first access command are set up to produce, during each
4 time interval, a binary signal opposite to the least
5 significant bit of the count number for the time interval
6 in progress;

7 the means of the controller for generating an
8 address at said first address output are set up to produce
9 an address equal to the first partial count number during
10 the time intervals respectively numbered from 0 to 2^N-1 ,
11 and equal to $2^{N-1}-2$ from which the first partial count
12 number is subtracted during the time intervals respectively
13 numbered from $2N$ to
14 $2^{N+1}-1$;

15 the means of the controller for generating the
16 second access command are set up to produce, during each
17 time interval, a signal equal to the least significant bit
18 of the time interval in progress; and

19 the means of the controller for generating an
20 address at said second address output are set up to produce
21 an address equal to the second partial count number during
22 the time intervals respectively numbered from 0 to 2^N-2 or
23 numbered $2^{N+1}-1$, and equal to $2^{N-1}-1$ from which the second
24 partial count number is subtracted during the time
25 intervals respectively numbered from 2^N to $2^{N+1}-1$, or
26 numbered 2^N-1 .

1 10. The device according to Claim 9, wherein the
2 controller comprises:

3 a first internal multiplexer having a first input
4 connected to receive the first partial count number, a
5 second input connected to receive the value, over $N-1$ bits,
6 of $2^{N-1}-2$ from which the first partial count number is
7 subtracted, a command input connected to receive the most
8 significant bit of the count number for the time interval
9 in progress, and set up to reproduce at an output connected
10 to the first address output of the controller the value
11 received on the first or second input of said first
12 internal multiplexer, when the value applied to the command
13 input of said first internal multiplexer is 0 or 1,
14 respectively; and

15 a second internal multiplexer having a first
16 input connected to receive the second partial count number,
17 a second input connected to receive the value, over N-1
18 bits, of $2^{N-1}-1$ from which the second partial count number
19 is subtracted, a command input connected to receive the
20 most significant bit of the count number for the time
21 interval in progress to which 1 is added, and set up to
22 reproduce at an output connected to the second address
23 output of the controller the value received at the first
24 or second input of said second internal multiplexer, when
25 the value applied to the command input of said second
26 internal multiplexer is 0 or 1, respectively.

1 11. The device according to Claim 6, wherein the
2 memories are instant read memories, the data read in each
3 memory being produced at the output of said memory in the
4 time interval during which the command input of said memory
5 receives a read access command and the address input of
6 said memory receives an address, and wherein the controller
7 comprises:

8 a cyclic counter of the time intervals of the two
9 consecutive sequences, set up to produce a number over N+1

10 bits, between 0 and $2^{N+1}-1$, for counting the time interval
11 in progress;

12 means for producing, during each time interval,
13 a first partial time interval count number over N-1 bits,
14 equal to the count number for the time interval in progress
15 from which the most significant bit and the least
16 significant bit have been removed;

17 means for producing, during each interval, a
18 second partial time interval count number over N-1 bits,
19 equal to the count number for the time interval in progress
20 to which 1 is added, then from which the most significant
21 bit and the least significant bit have been removed;

22 means for generating at said second switching
23 command output the second switching signal in the form of
24 a binary signal equal to 0 when the count number for the
25 time interval in progress, reduced to the N least
26 significant bits, is equal to 2^N-1 , and equal to 1
27 otherwise;

28 means for generating at a first address output
29 connected to the address input of a first of the two
30 memories an address equal to the first partial count number
31 during the time intervals respectively numbered from 0 to
32 2^N-2 , and equal to $2^{N-1}-1$ from which the second partial

33 count number is subtracted during the time intervals
34 respectively numbered from 2^N to $2^{N+1}-2$;

35 means for generating at a second address output
36 connected to the address input of a second of the two
37 memories an address equal to the second partial count
38 number during the time intervals respectively numbered from
39 0 to 2^N-2 , and equal to $2^{N-1}-1$ from which the first partial
40 count number is subtracted during the time intervals
41 respectively numbered from 2^N to $2^{N+1}-2$;

42 means for generating at a first access command
43 output connected to said first memory a first binary access
44 command, for the time intervals numbered other than 2^N-1
45 and $2^{N+1}-1$, equal to:

46 $[^cC(0) \text{ EXCL_OR } C(N)] \text{ OR } ^c[\text{second switching signal}]$,

47 where:

48 $C(0)$ is the least significant bit of the time interval in
49 progress,

50 $C(N)$ is the most significant bit of the time interval in
51 progress,

52 EXCL_OR is the "exclusive OR" binary operator,

53 cX designates the opposite value to the binary value X;

54 means for generating at the second access command
55 output connected to said second memory a second binary

56 access command equal to $[C(0) \text{ EXCL_OR } C(N)] \text{ OR } ^c[\text{second}$
57 switching signal], for the time intervals respectively
58 numbered other than 2^N-1 and $2^{N+1}-1$;

59 means for generating at the first switching
60 command output a binary signal opposite to the first access
61 command;

62 each of the two memories being in write or read
63 access mode when the corresponding access command is equal
64 to 0 or 1, respectively;

65 the first and second multiplexer each being set
66 up to instantaneously reproduce at the output of said
67 multiplexer a signal applied to the first or second input
68 of said multiplexer, when the switching signal applied to
69 the command input of said multiplexer is equal to 0 or 1,
70 respectively.

1 12. The device according to Claim 11, wherein:

2 the means of the controller for generating the
3 first access command are set up to produce, during each
4 time interval, a binary signal equal to $[^cC(0) \text{ EXCL_OR}$
5 $C(N)]$;

6 the means of the controller for generating the
7 second access command are set up to produce, during each

8 time interval, a binary signal opposite to the first access
9 command;

10 the means for generating an address at the first
11 address output are set up to produce a signal equal to the
12 first partial count number during the time intervals
13 respectively numbered from 0 to 2^N-1 , and equal to $2^{N-1}-1$
14 from which the second partial count number is subtracted
15 during the time intervals respectively numbered 2^N to
16 $2^{N+1}-1$;

17 the means for generating an address at the second
18 address output are set up to produce a signal equal to the
19 second partial count number during the time intervals
20 respectively numbered from 0 to 2^N-1 , and equal to $2^{N-1}-1$
21 from which the first partial count number is subtracted
22 during the time intervals respectively numbered 2^N to
23 $2^{N+1}-1$.

1 13. The device according to Claim 12, wherein the
2 controller comprises:

3 a first internal multiplexer having a first input
4 connected to receive the first partial count number, a
5 second input connected to receive the value, over N-1 bits,
6 of $2^{N-1}-1$ from which the second partial count number is

7 subtracted, a command input connected to receive the most
8 significant bit of the count number for the time interval
9 in progress, and set up to reproduce at an output connected
10 to the first address output of the controller the value
11 received at the first or second input of said first
12 internal multiplexer, when the value applied to the command
13 input of said first internal multiplexer is 0 or 1,
14 respectively; and

15 a second internal multiplexer having a first
16 input connected to receive the second partial count number,
17 a second input connected to receive the value, over N-1
18 bits, of $2^{N-1}-1$ from which the first partial count number is
19 subtracted, a command input connected to receive the most
20 significant bit of the count number for the time interval
21 in progress, and set up to reproduce at an output connected
22 to the second address output of the controller the value
23 received at the first or second input of said second
24 internal multiplexer, when the value applied to the command
25 input of said second internal multiplexer is 0 or 1,
26 respectively.

1 14. The device according to Claim 1, wherein the
2 memories are instant read memories, the data read in each

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3 memory being produced at the output of said memory in the
4 time interval during which the command input of said memory
5 receives a read access command and the address input of
6 said memory receives an address.

1 15. A method of data storage comprising the following
2 steps each carried out within successive time intervals of
3 two consecutive sequences of $2N$ time intervals, N being an
4 integer greater than 1:

5 issuing a data from a data source to two random
6 access memories, each memory having at least $2N-1$ locations
7 for storing data at respective addresses, while issuing
8 directly said data to a multiplexer further connected to
9 respective data outputs of the two memories;

10 for at least time intervals distinct from the
11 boundaries of the two sequences, issuing alternate read and
12 write access commands respectively to each of the two
13 random access memories, a write access command being issued
14 to one of the memories while a read access command is
15 issued to the other memory and vice versa;

16 issuing to each memory, increasing addresses
17 during one of the two sequences and decreasing addresses
18 during the other sequence, such that, for at least time
19 intervals distinct from boundaries of the two sequences,
20 each memory receives the same address in the course of two
21 consecutive time intervals of each sequence during which

22 said memory receives a read access command and then a write
23 access command; and
24 issuing switching signals to the multiplexer, the
25 switching signals causing the multiplexer to reproduce on
26 an output either the data received directly from the data
27 source or the data received from one of the two memories,
28 as selected by the switching signals, so that in the course
29 of each sequence, data is produced which originates from
30 the source in a reverse chronological order from the
31 chronological order of arrival of said data from the
32 source.

1 16. A data storage device, comprising:
2 two random access memories for storing data at
3 respective addresses, a data input connected to a data
4 source, a command input, an address input and an output;
5 a multiplexor having first and second data inputs
6 respectively connected to the data outputs of the two
7 memories and an output reproducing data present at one of
8 said first and second data inputs;
9 a controller for issuing command signals to the
10 command inputs of the two memories, address signals to the
11 address inputs of the two memories and switching signals
12 to the multiplexor; and
13 a logic device to sample the output of the
14 multiplexor and produce output data,
15 wherein the controller issues:
16 alternate read/write command signals to the two
17 random access memories so as to write data to one memory
18 while reading data from another memory;
19 address signals to the address inputs of the two
20 random access memories, while alternate read/write command
21 signals are provided, comprising increasing address values
22 followed by decreasing address values; and

23 switching signals to the multiplexor to
24 alternately select between the two random access memories
25 with respect to data read from the memories.

1 17. The data storage device of claim 16 further
2 comprising:
3 a second multiplexor having first and second data
4 inputs respectively connected to the outputs of the first
5 multiplexor and a source of data and an output reproducing
6 data present at one of said first and second data inputs;
7 wherein the controller issues switching signals
8 to the second multiplexor to selectively output data
9 received from the source of data instead of data received
10 from the multiplexor.

1 18. A method for LIFO data storage comprising:
2 alternately writing received data into first and
3 second memories;
4 oppositely alternately reading previously written
5 data from the first and second memories; and
6 selecting addresses in the first and second
7 memories for the writing/reading of data to sequentially
8 increment through the memories during a first time interval
9 and then sequentially decrement through the memories during
10 an immediately following second time interval.

1 19. The method of claim 18 wherein the selection of
2 addresses selects an address in one of the memories in the
3 first time interval for writing data into the memory and
4 then selects the same address in the same one of the
5 memories in the second time interval for reading data from
6 the memory.

1 20. The method of claim 18 wherein the oppositely
2 alternatively reading includes alternately selecting
3 between the first and second memories to output read data.

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1 21. The method of claim 20 wherein the output read
2 data is produced in a reverse chronological order to that
3 with which it was received.